ECE 3223
Homework 3

Fall 1997 Dr. Havlicek

Design a 4-bit 3-point median filter in hardware.

Inputs:	**X_{in}:**	4-bit integer giving the value of the next input sample.
	DAV_{in}:	This signal is high when X_{in} is valid and can be latched on the next rising edge of CLK.
Outputs:	**MEDIAN:**	4-bit unsigned integer; the median of the last three inputs received
	DAV_{out}:	This signal is high when the MEDIAN output is valid.

Design the circuit so that the MEDIAN output is valid and DAV_{out} is asserted during the next clock cycle after each new input arrives.
Use these devices:

Quantity	Type
3	4-bit registers
3	4-bit comparators
4	Quad 2×1 MUX
as needed	Combinational logic and individual flip-flops.

NOTE: This design does NOT require a control unit.