ECE 3223
Homework 4

Fall 1997 Dr. Havlicek

Revise your solution to HW3 so that only TWO comparators are used. The input and output signals of this design are the same as those for HW3, except that the MEDIAN output will be ready and DAV_{out} will be asserted during the SECOND clock cycle after DAV_{in} is asserted.

Use these devices:

Quantity	Type
5	4-bit registers
2	4-bit comparators
5	Quad 2×1 MUX
as needed	Combinational logic and individual flip-flops.

NOTE: This design DOES require a control unit. Design the control unit using D flip-flops and combinational logic as needed.